Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-2. (canceled)

3. (currently amended) The integrated-circuit device in claim [[2]] 13, in which the electric current passes the channel region upon a biasing voltage being applied between the source terminal and the drain terminal, and the magnitude of the current in the channel region is controllable with a biasing voltage at the gate terminal.

4. (currently amended) The integrated-circuit device in claim [[2]] 13, in which the substrate is p-type silicon.

5. (currently amended) The integrated-circuit device in claim [[2]] 13, further comprising an n-type buried layer (NBL).

6. (previously presented) The integrated-circuit device in claim 5, in which the NBL is doped with antimony.

7. (currently amended) The integrated-circuit device in claim [[2]] 13, in which the first region is formed by an epitaxial growth technique.

8. (original) The integrated-circuit device in claim 7, in which the epi layer is n-type.

9. (currently amended) The integrated-circuit device in claim [[2]] 13, in which the substrate is a bonded wafer.

10-12. (canceled)

13. (currently amended) An integrated-circuit device, comprising:

a substrate, having a top surface and a bottom surface; and

a vertical JFET, including:

a first and second gate regions in a first region near the top surface of the substrate, each having a top surface, a bottom surface and a side surface;

the side surfaces of the first and second gate regions being substantially parallel to each other and substantially perpendicular to the top surface of the substrate;

the top surface of the first gate region being electrically communicable to a gate terminal;

a channel region in the first region, between the first and the second gate regions having side surfaces adjacent to the side surfaces of the gate regions, a top surface, and a bottom surface;

the top surface of the channel region electrically communicable to a source terminal, the bottom surface of the channel region electrically communicable to a drain terminal;

the gate terminal, the source terminal, and the drain terminal being near the top surface of the substrate;

the JFET operable to pass an electric current between the source terminal and the drain terminal, the electric current flowing in the channel region in a direction vertical to the top and bottom surfaces of the channel region;

the first gate region having a pill-box shape with a substantially flat top surface and bottom surface, and a side surface substantially perpendicular to the top and bottom surfaces;

the channel region having a ring shape enclosing the first gate region, a bottom surface substantially coplanar to the bottom surface of the first gate region and a top surface substantially coplanar to the top surface of the first gate region;

the second gate region having a ring shape enclosing the channel region, a bottom surface substantially coplanar to the bottom surface of the first gate region and a top surface substantially coplanar to the top surface of the first gate region; and

a drain plug region [[has]] having a ring shape enclosing the second gate region, a bottom surface substantially coplanar to the bottom surface of the first gate region and a top surface substantially coplanar to the top surface of the first gate region.

14. (original) The integrated-circuit device in claim 13, in which gate-, source-, and drain-contact areas are formed on the top surfaces of the gate-, channel-, and drain-region respectively.

15. (original) The integrated-circuit device in claim 14, in which metal leads are formed connecting a gate contact area to a gate terminal, a source contact to a source terminal, and a drain contact area to a drain terminal.